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Comparative Analysis of Low-Power Radiation-Tolerant SRAM Cells for Aerospace Applications

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Abstract:

Modern aerospace electronics demand the implementation of SRAM design structures that have minimal power dissipation, high reliability, and excellent soft error resilience when subjected to radiation. Traditional SRAMs are associated with the problem of leakage current, small static noise margin (SNM) and low reliability in nanometer-scale CMOS technologies. In this research paper, a comparison study between traditional 6T SRAM, Dice SRAM, We-Quatro SRAM, and the proposed Deep Radiation Flexible (DRF) 10T SRAM is done. The DRF 10T SRAM structure proposed in this study is designed to minimize leakage power dissipation, enhancing radiation tolerance, and improving reliability during read and write operations. All SRAM designs are designed and simulated using Cadence Virtuoso in UMC 55nm CMOS technology. The performance comparison was done based on leakage power, delay, SNM, and soft error recovery rate. Comparison reveals that the proposed architecture is more resilient to soft errors and has better signal integrity than other existing architectures. Moreover, the DRF 10T SRAM has been successfully tested under high-frequency operations and process variability. The results thus obtained suggest that the proposed SRAM architecture offers a good compromise between power consumption and radiation hardness.

Keywords: SRAM, 10T SRAM, Radiation Tolerance, CMOS Technology, Low Power, Static Noise Margin, Soft Error Resilience.

1. Introduction

Static Random Access Memory (SRAM) is considered one of the crucial elements of modern computing systems owing to its fast speed, low access time, and CMOS technology compatibility. SRAM cells are widely applied in cache memories, embedded processing units, aerospace electronic systems and portable systems. The continuous shrinking of CMOS technology to nanometer dimensions poses substantial problems for SRAM cells, including leakage current, SNM degradation, process variation and radiation-induced soft error vulnerability [1-3].

High-energy particles such as alpha particles and cosmic rays may interfere with the charged state within the SRAM cells in the field of aerospace technology. Such interference causes single event upsets (SEUs) or transient faults. Conventional 6T SRAM is characterized by low radiation immunity and poor write margin at nanometer level. In recent times, various

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radiation-hardened designs including Dice SRAM and We-Quatro SRAM have been suggested to enhance soft error resistance. The radiation-hardened SRAM suffers from greater power dissipation and delay problems [4-6].

To circumvent the above challenges, this study offers an analytical comparison between traditional 6T SRAM, Dice SRAM, We-Quatro SRAM and the proposed Deep Radiation Flexible (DRF) 10T SRAM cell [7-8]. This research paper proposes the design of a novel 10T SRAM cell capable of providing a low power leakage, high reliability of read/write operation, increased SNM and high radiation soft error recovery capability. The design and simulation of the SRAM cells have been performed in Cadence Virtuoso using UMC 55 nm CMOS technology [9-10].

2. Related work

There are several types of SRAM structures designed for achieving better power efficiency, stability and soft error tolerance. The common type of SRAM structures is the 6T SRAM, which is widely used due to its small size and fast operations. However, such SRAMs have weak read stability, high leakage power consumption and radiation-sensitive soft errors.

In order to increase SEU immunity, the Dice SRAM scheme was developed, which included redundant cells and recovery feedback systems. The Dice SRAM scheme can offer better protection against SEUs. But due to the high transistor count, its design requires more power and area. Likewise, the We-Quatro SRAM scheme offers enhanced radiation recovery capability by using extra feedback transistors and isolation of storage cells. Despite this, the We-Quatro SRAM scheme suffers from more delay and energy usage while operating dynamically.

Many researches have even put forward SRAM architectures having 8 and 10-transistors to provide stable reading/writing and minimize the leakage current. These architectures concentrate on isolating the read path, minimizing the disturbance in reading operations and increasing SNM values. Nevertheless, many SRAM structures available today suffer from disadvantages like high write time, lower speed and inadequate radiation hardness.

Thus, there exists a need to design an SRAM design that ensures low power dissipation, SNM improvement, reduced delay and also an effective recovery from radiation effects. In this paper, a DRF 10T SRAM cell has been introduced and compared with traditional SRAM designs in order to ensure robust and energy-efficient operation of memory circuits in space.

3. Methodology

The proposed Deep Radiation Flexible (DRF) 10T SRAM cell is designed to achieve a low power dissipation, good stability and radiation resistance capability to ensure efficient operation of aerospace electronic systems. The proposed cell includes 10 transistors, which include the cross-coupled inverters, the access transistor and some recovery transistors. The incorporation of more NMOS and PMOS transistors can increase write capability, read stability, and radiation recovery capability.

The suggested DRF 10T SRAM cell works through two distinct paths: a read path and a write path, which helps reduce the chances of

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any read disturbances. When writing to the cell, the word line accesses the cell via its access transistors, thereby facilitating the transmission of the input data through the bit line into the internal storage nodes. The use of pass transistors makes it easier to write due to enhanced logic switching and increase in write noise margin. On reading from the cell, no disturbance occurs to the internal storage nodes since they are isolated from the read path.

In order to increase radiation immunity, additional PMOS recovery transistors are used in the SRAM design. In case an energetic particle impacts on a susceptible node leading to the disruption of its voltage levels, the remaining internal nodes initiate the recovery transistors, thus restoring the impacted node to its initial state. The process significantly reduces the occurrence of SEUs.

This new design of the 10T SRAM structure shown in figure 1 was proposed, developed, and simulated in Cadence Virtuoso using UMC 55nm CMOS process technology. The performance of the suggested SRAM cell was assessed based on its power consumption, read delay, write delay, static noise margin, and radiation recovery capacity. From comparison of the suggested SRAM structure with 6T SRAM, Dice SRAM, and We-Quatro SRAM, it is evident that the proposed DRF 10T SRAM cell offers superior stability and reliability.

Figure 2 illustrates the schematic diagram of the suggested SRAM cell, which consists of 10 transistors, providing improved stability, leakage power minimization, and effective reading and writing operations.

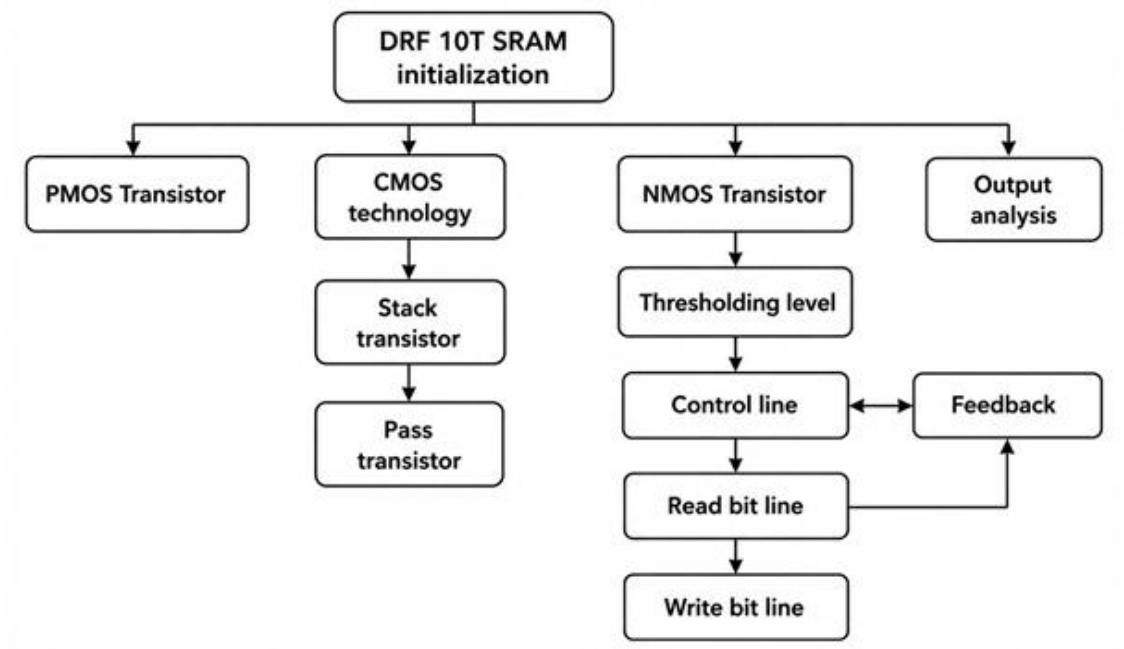

Figure 1: Block Diagram

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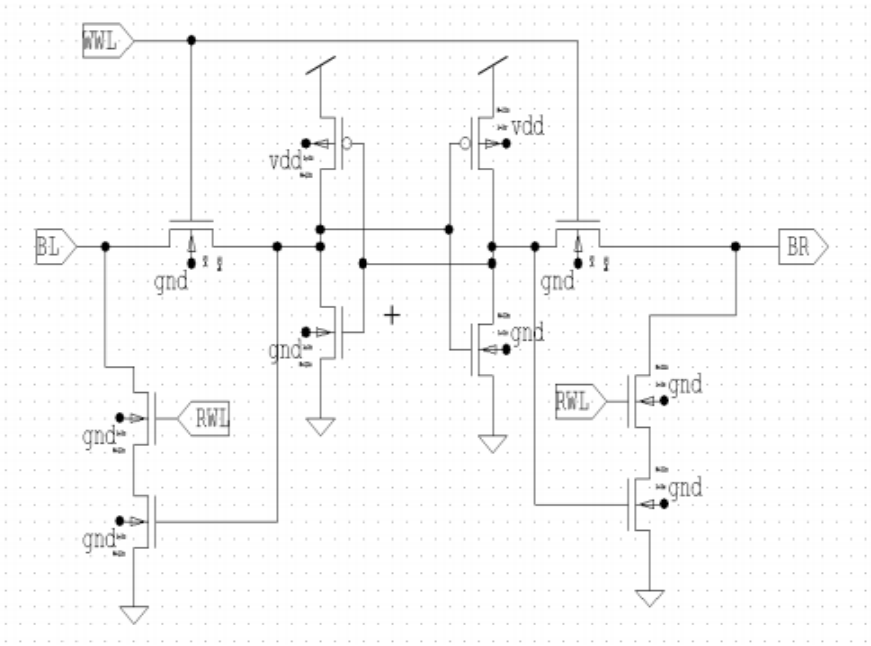

Figure 2: Architecture - DRF 10T SRAM cell

4. Results and Discussion

The performance of the suggested SRAM cell was assessed based on its power consumption, read delay, write delay, static noise margin, and radiation recovery capacity. From comparison of the suggested SRAM structure with 6T SRAM, Dice SRAM, and We-Quatro SRAM, it is evident that the proposed DRF 10T SRAM cell offers superior stability and reliability.

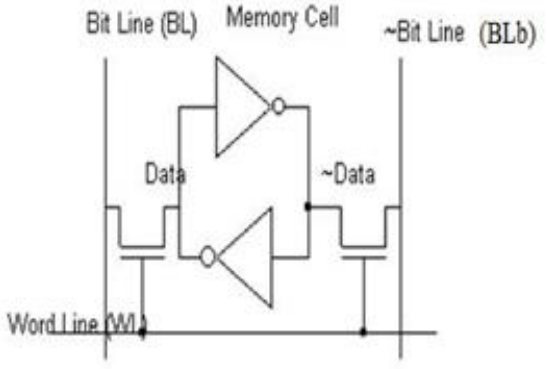

Figure 3: General structure of the SRAM cell

Figure 3 shows the fundamental arrangement of the SRAM memory cell with cross-coupled inverters linked via bit lines (BL and BLb) and managed via the word line (WL). The complementary nature of storing data guarantees successful read and write functions, ensuring consistent storage of logic values in the memory cell.

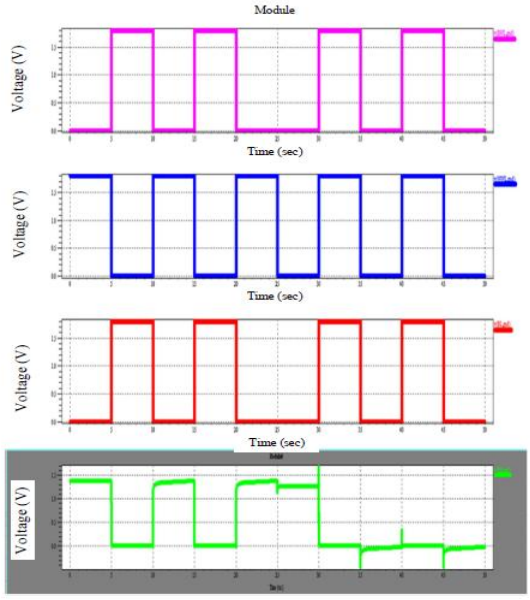

Figure 4: Simulation of 12T SRAM

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Figure 4 describes the write instability phenomenon experienced by conventional 12T SRAM cell due to high frequency operations. From the waveform, it can be seen that the output node "A" has been successfully pulled down to logic '0' using N1 transistor, whereas node "B" has been pulled up by NMOS transistor N2. Due to weak pulling behavior of NMOS transistor, there has been delay in the rising voltage at node "B", which could not achieve full logic '1' state efficiently. Thus, there is a lot of propagation delay associated with the writing operation. Consequently, the writing task cannot be completed in the given switching period at high frequencies.

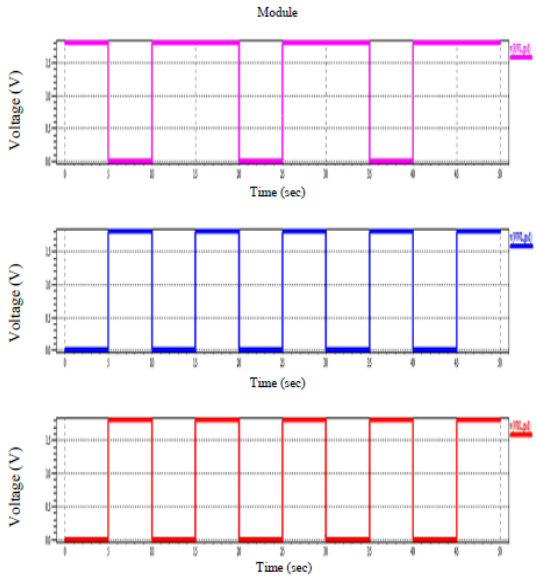

Figure 5: Simulation of Dice SRAM

The waveforms shown in Figure 5 represent the transient switching behavior of the Dice SRAM cell in normal read/write mode. There is an appropriate transition from a high state to a low state and vice versa. This clearly indicates the stable synchronization of the control signals and the internal memory nodes. The memory nodes store the data efficiently and do not lose it even after several switching operations. This shows the efficient performance of the memory circuit. Thus, it can be concluded that the waveforms obtained prove the stable performance of the proposed SRAM cell.

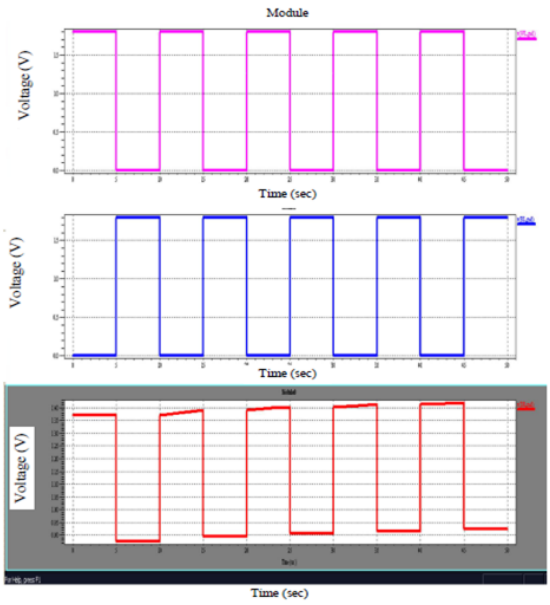

Figure 6 : Simulation of We-Quatro SRAM cell

Figure 6 shows the radiation error recovery performance of the We-Quatro SRAM configuration for a high energy particle hit condition. The hit of the particle on node "B" causes an instant transition of the stored binary state at node "B" from logic "1" to logic "0", creating a disturbance in the memory cell. As a result of the disturbance at node "B", transistor P3 gets ON for a very short duration of time, which also causes disturbance at node "C". However, node "A" does not show any disturbance since node "B" is decoupled from other storage nodes by transistors N5 and N2. The error recovery transistors P2 and N7 are able to recover nodes "B" and "C" back to their initial binary states.

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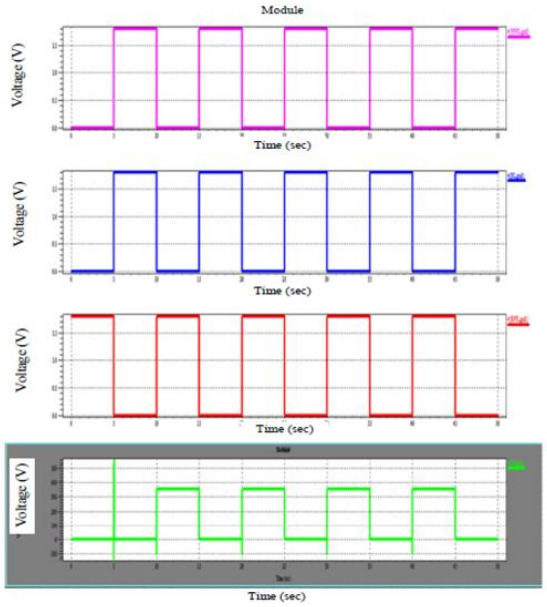

Figure 7: Simulation of DRF 10T SRAM

Figure 7 depicts the read and write operation properties of the designed DRF 10T SRAM cell under dynamic operations. The waveforms recorded demonstrate steady state changes and reliable performance during the read and write operations. In comparison to standard SRAM designs, the designed DRF 10T SRAM cell possesses superior operational speed and better operational performance. The rapid voltage changes and minimal signal variations suggest superior signal fidelity and efficient data storage property. In addition, the designed structure provides low power consumption during the switching operations because of the optimized transistor configuration. Hence, the analysis of waveforms proves the superiority of the designed DRF 10T SRAM cell.

Table 1 Parameters comparison of SRAMs

SRAM cells parameters	Proposed	12TSRAM (RHBD) (Prasad, et al. 2021)	We-Quatro (Kim and Chang 2017)	Dice (12T) (Prasad, et al. 2021)
Total power (µW)	0.83	0.981	2.025	1.36
Static power (pW)	20.2	26.25	32.32	28.15
Write delay (pS)	13.5	14.04	17.20	16.43
Read delay (pS)	82.9	83.21	70.56	63.25
Critical charge (fC)	12.2	12.15	9.22	6.25
Area (µm^2)	4.1	4.29	4.21	4.5

As seen from the comparison, the suggested DRF SRAM cell provides significantly higher performance compared to RHBD 12T SRAM cell, We-Quatro SRAM, and Dice SRAM architectures. Specifically, the suggested cell consumes the least total power (0.83 µW) and low static power (20.2 pW), which indicates high energy efficiency with minimal leakage currents. In addition, the write delay has been reduced to 13.5 ps, implying faster operation and improved switching ability. However, while the proposed cell has marginally high read delay compared with Dice and We-Quatro SRAM cells, it possesses significantly better critical charge capability of 12.2 fC, which suggests better tolerance to radiation-caused soft errors. Furthermore, the proposed cell uses the smallest chip area of 4.1 µm2, making it more efficient concerning the chip space

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used. Hence, as can be seen, the proposed DRF SRAM cell offers an excellent compromise between power consumption, stability, radiance tolerance, and chip size.

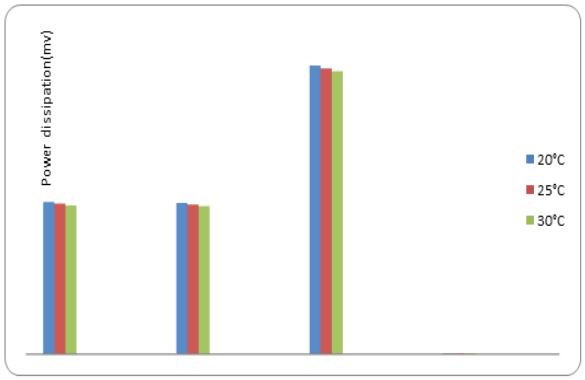

Figure 8: Power Dissipation at Different Temperature

From figure 8, it can be seen from the graph that there is negligible variation in the power dissipation value of the DRF 10T SRAM cell at different operating temperatures, which suggests that the leakage current value of the new SRAM architecture is low at different temperatures. Therefore, it can be said that the power dissipation behavior of the DRF 10T SRAM cell is highly reliable and consumes less energy at different temperatures.

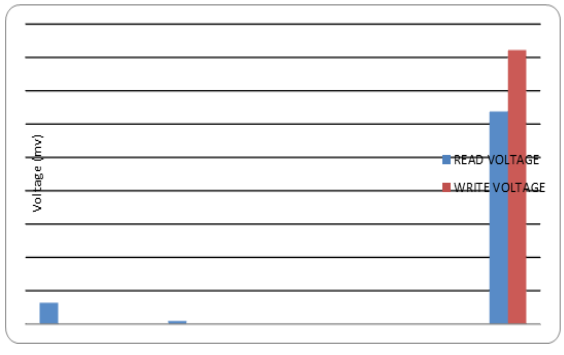

Figure 9: Read and Write Voltages at Particular Node

From figure 9, it can be seen that the comparison is made between the read voltage and write voltage properties during memory functions. From the graph, it can be observed that the write voltage is larger than the read voltage, which indicates better write performance and superior data transition performance in the proposed SRAM design. This suggests that the proposed SRAM design is more reliable and efficient due to its superior voltage property.

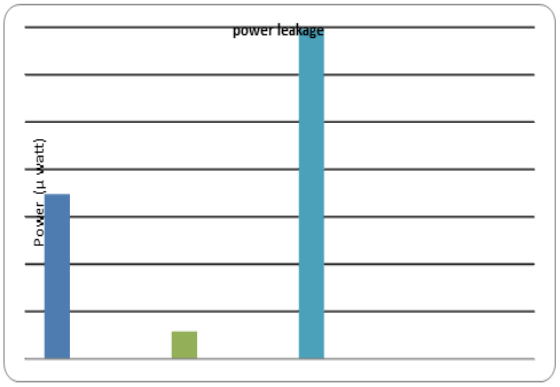

Figure 10: Overall power leakage

The power consumption in figure 10 reveals that the proposed design is capable of lowering its power consumption level relative to existing SRAM designs. The plot suggests that the proposed SRAM model consumes less power because of its efficient transistor arrangement and effective standby power consumption control. Lowering power consumption makes the design more energy-efficient and prevents wastage of power when the SRAM is not in use. Hence, the proposed DRF 10T SRAM design provides better low-power performance and reliability.

5. Conclusion

This work conducted a comparison analysis of radiation-tolerant low-power SRAM memory cells using Cadence Virtuoso software at UMC 55 nm CMOS process technology. This study proposed DRF-based

10T SRAM memory cell that aims to improve read/write stability, minimize leakage power, and increase radiation recovery from soft errors. Results showed that the proposed radiation-tolerant SRAM memory had a better performance in total power reduction, static leakage power reduction, and faster writing operations when compared to existing SRAM memory cells. Radiation recovery analysis validated the effective mitigation of SEU events by the proposed feedback recovery feature of the DRF SRAM structure. Also, the proposed SRAM memory structure provided stable reading and writing operations with increased signal integrity and low disturbance during high-speed operations. Furthermore, comparative analysis validated the effectiveness of improved critical charge tolerance and efficient use of area. These findings demonstrate the successful improvement of power efficiency, operational stability, and radiation resistance provided by the proposed DRF 10T SRAM memory structure.

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